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CLAIMS

1. A process for treating substrates (50) for the microelectronics or optoelectronics industry, comprising on at least one of their faces a working layer (52) in which components are intended to be formed, this process comprising a step of chemical-mechanical polishing on the free surface (54) of the working layer (52), which also comprises a step of annealing under a reductive atmosphere (100, 100A, 100B, 100C, 101D, 102D), before the polishing step (200, 200A, 200B, 200C, 200D).
2. The process as claimed in claim 1, wherein the step of annealing under a reductive atmosphere is carried out in less than three minutes, preferably in less than sixty seconds and even more preferably in less than thirty seconds.
3. The process as claimed in either of the preceding claims, wherein the step of annealing under a reductive atmosphere is carried out at a temperature of between 1100°C and 1300°C, and preferably between 1200°C and 1230°C.
4. The process as claimed in one of the preceding claims, which also comprises, after the polishing step (200, 200A, 200B, 200C, 200D), a step (310A, 312B, 312C) of oxidizing the working layer (52) over at least a portion of its thickness.
5. The process as claimed in one of the preceding claims, which also comprises, before the polishing step (200, 200A, 200B, 200C, 200D), a step (311B, 311C) of oxidizing the working layer (52) over at least a portion of its thickness.
6. The process as claimed in either of claims 4 and 5, which also comprises at least one oxide removal step (330A, 331B, 332B, 331C, 332C).
7. The process as claimed in one of claims 4 to 6, which also comprises at least one heat treatment step (320A, 321B, 322B, 321C, 322C), the step of oxidizing

the working layer (52) being carried out before the end of each heat treatment step (320A, 321B, 322B, 321C, 322C), in order to protect the rest of the working layer (52).

5 8. The process as claimed in one of the preceding claims, which also comprises a step of annealing under a reductive atmosphere (102D) after the polishing step (200, 200A, 200B, 200C, 200D).

9. The process as claimed in one of the preceding
10 claims, which comprises a step of implanting atoms under one face of a wafer, in an implantation zone, a step of placing the face of the wafer, which has undergone the implantation, in intimate contact with a support substrate, and a step of cleaving the wafer in
15 the implantation zone, in order to transfer some of the wafer onto the support substrate and form a thin film or a thin layer thereon, this thin film or this thin layer constituting the working layer (52) which is then subjected to the steps of annealing under a reductive
20 atmosphere (100, 100A, 100B, 100C, 101D, 102D) and of polishing (200, 200A, 200B, 200C, 200D).

10. The process as claimed in one of the preceding claims, wherein the working layer (52) consists of a semiconductor.

25 11. The process as claimed in claim 10, wherein the semiconductor is silicon.

12. The process as claimed in one of the preceding claims, wherein the reductive atmosphere comprises hydrogen.

30 13. The process as claimed in one of the preceding claims, wherein the reductive atmosphere comprises argon.